

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant :	Hidetoshi Nishikawa	Art Unit :	2819
Serial No. :	10/567,991	Examiner :	Jason Crawford
Filed :	February 9, 2006	Confirmation No.:	5510
		Notice of Allowance Date:	April 3, 2007
Title :	SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE		

MAIL STOP ISSUE FEE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO NOTICE OF ALLOWANCE

In response to the Notice of Allowance mailed April 3, 2007, enclosed are a completed issue fee transmittal form PTOL-85b. The required issue fee and publication fee in the amount of \$1700 are being paid concurrently herewith on the Electronic Filing System (EFS) by way of Deposit Account authorization.

COMMENTS ON REASONS FOR ALLOWANCE

The Examiner's allowance of the claims is appreciated. The Applicant submits the following comments concerning the Examiner's Reasons for Allowance cited in the Notice of Allowability. It is the subject matter of each claim as a whole that is patentable, not any particular feature recited in the claim(s). The Applicant does not concede that the reasons for allowance given by the Examiner are the only reasons that make the claims allowable and does not make any admission or concession concerning the Examiner's statement.

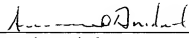
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Attorney's Docket No.: 19415-007US1 / PCT-04R-
166/US

Please apply any additional charges or credits to our Deposit Account No. 06-1050.

Respectfully submitted,

Date: 7/3/07



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